HOT SWITCHABLE VOLTAGE BUS FOR IDDQ CURRENT MEASUREMENTS

TECHNICAL FIELD

[0001] The present invention relates in general to integrated circuits. More particularly, the present invention is directed to a voltage island system including a hot-switchable voltage bus for IDDQ current measurements.

BACKGROUND ART

[0002] Voltage islands are often designed into and implemented on integrated circuit chips to allow active and standby power reduction by changing the supply voltages to individual voltage islands. Voltage islands have also been implemented to reduce noise via supply isolation. The voltage island concept can reduce power consumption substantially by allowing designers to build, for example, processors that vary their voltages across a chip. For example, a single system-on-a-chip processor could be built to run one voltage in one or more areas of the chip, such as a processor core, a different voltage in other areas of the chip, and to switch off the voltage to areas of the chip that are not in use.

[0003] An example of a voltage island system 10 is illustrated in FIG. 1. As shown, the voltage island system 10 includes a plurality of voltage islands V1, V2, ..., Vn and a corresponding plurality of on-chip header devices H1, H2, ..., Hn for selectively providing a voltage VDDg to the voltage islands V1, V2, ..., Vn in response to header control signals x1, x2, ..., xn, respectively. A global

VDDg power supply 12 provides power to the header devices H1, H2, ..., Hn via a VDDg power distribution grid/bus 14.

[0004] In today's voltage island implementations, none, some, or all voltage islands of a chip can be powered up during test. One test, for example, involves measuring the quiescent current (IDDQ) in the VDD supply (e.g., VDDg power supply12 in FIG. 1). This test is performed by measuring the current of a chip at the power supply (or ground) or chip terminals, typically after applying test patterns to the voltage islands via a scan chain. IDDQ testing depends on the fact that some defects in the chip cause additional quiescent current. By comparing the IDDQ value of the device under test (DUT) to a pass/fail value, a determination can be made as to whether the DUT is defective or not. The pass/fail value may be determined using statistics from individual wafers/lots, or may be determined using other known methods.

[0005] IDDQ testing has been shown to be effective in screening out a class of reliability problems. However, the effectiveness of IDDQ testing decreases as the level of subthreshold leakage or background current increases. For example, if the IDDQ test is capable of finding defects that cause a 10% increase in IDDQ, on a chip that typically measures 1mA during IDDQ test, a defect that generates 0.1 mA of additional current can be detected. On a chip that typically measures 1 A during IDDQ test, however, a defect must generate 100mA of current to be detected. Thus, on a chip that typically generates 1 A IDDQ, a defect that generates 0.1 mA of additional current will not be detected, and may result in a possibly unexposed reliability problem.

[0006] When IDDQ measurements are performed in the voltage island system 10 of FIG. 1 using the global VDDg power supply 12, some amount of background current is measured. If this level of background current could be reduced in some manner, smaller defects that produce smaller defect currents could be more easily detected. Accordingly, there exists a need for a method/apparatus for increasing the effectiveness of IDDQ testing by limiting the component of background current in the measurement. In addition, there

exists a need for a method/apparatus for locating IDDQ defects in a voltage island system.

[0007] During IDDQ testing, voltage islands are often turned off/on in various configurations while applying the same test pattern. In the voltage island system 10 of FIG. 1, for example, the voltage islands V1, V2, ..., Vn may be tested using the same test pattern with all or none of the voltage islands turned on, with selected groups of the voltage islands turned on, or with single voltage islands turned on. Unfortunately, the same test pattern must be reapplied by the tester each time a different set of the voltage islands V1, V2, ..., Vn is tested, which uses test time inefficiently. This occurs because a voltage island loses state when it is turned off (i.e., not powered). Accordingly, there is a need for a method/apparatus for reducing the time required for IDDQ testing.

DISCLOSURE OF THE INVENTION

[0008] The present invention provides a hot-switchable voltage bus for IDDQ current measurements. In accordance with the present invention, an integrated circuit (IC) can be broken up into voltage islands for IDDQ testing. A quiescent voltage bus (VDDq) is included in the IC. Voltage islands can be hot-switched between the IC power busses and VDDq to facilitate IDDQ testing.

[0009] A first aspect of the present invention is directed to a hot-switchable voltage bus for IDDQ measurement, comprising: a global voltage bus; a quiescent voltage bus, separate from the global voltage bus; at least one voltage island; and a system for selectively connecting each voltage island to the quiescent and global voltage busses during IDDQ testing.

[00010] A second aspect of the present invention is directed to a method for IDDQ testing, comprising: hot-switching at least one voltage island between a global power bus and a quiescent voltage bus; and performing IDDQ testing on the at least one voltage island.

[00011] A third aspect of the present invention is directed to a method, comprising: hot-switching at least one voltage island between a plurality of different voltage busses, wherein each voltage island does not lose state during the hot-switching.

[00012] A fourth aspect of the present invention is directed to a method for monitoring power consumption, comprising: connecting at least one voltage island to a quiescent voltage bus; and monitoring power usage at a VDDq power supply connected to the quiescent voltage bus for the at least one voltage island.

[00013] The exemplary aspects of the present invention are designed to solve the problems herein described and other problems not discussed, which are discoverable by a skilled artisan.

BRIEF DESCRIPTION OF THE DRAWINGS

[00014] These and other features of this invention will be more readily understood from the following detailed description of the various aspects of the invention taken in conjunction with the accompanying drawings in which:

[00015] FIG. 1 illustrates a voltage island system in accordance with the prior art.

[00016] FIG. 2 illustrates an embodiment of a voltage island system including a hot-switchable voltage bus for IDDQ current measurements in accordance with the present invention.

[00017] FIGS. 3 and 4 illustrate an example of a hot-switching process that can be carried out in accordance with the present invention.

[00018] FIGS. 5 and 6 illustrate another example of a hot-switching process that can be carried out in accordance with the present invention.

[00019] FIG. 7 illustrates a voltage island system including a plurality of voltage sensors in accordance with the present invention.

[00020] FIG. 8a and 8b illustrate the location of an IDDQ defect using voltage sensors in accordance with the present invention.

[00021] It should be noted that the drawings are merely schematic representations, not intended to portray specific parameters of the invention. The drawings are intended to depict only typical aspects of the invention, and therefore should not be considered as limiting the scope of the invention. In the drawings, like numbering represents like elements.

BEST MODE FOR CARRYING OUT THE INVENTION

[00022] The present invention addresses the above-mentioned problems, as well as others, by providing a voltage island system including a hot-switchable voltage bus for IDDQ current measurements.

[00023] Referring now to FIG. 2, there is illustrated a voltage island system 100 in accordance with the present invention. As shown, the voltage island system 100 includes a plurality of voltage islands V1, V2, ..., Vn, a global power system 102, and a quiescent power system 104. The global power system 102 includes a first plurality of on-chip header devices H1, H2, ..., Hn for selectively providing a voltage VDDg to the plurality of voltage islands V1, V2, ..., Vn in response to first header control signals x1, x2, ..., xn, respectively. A global VDDg power supply 106 provides power to the header devices H1, H2, ..., Hn via a VDDg power distribution grid/bus 108. The quiescent power system 104 includes a second plurality of on-chip header devices H1q, H2q, ..., Hnq for selectively providing a quiescent voltage VDDq to the plurality of voltage islands V1, V2, ..., Vn in response to second header control signals x1q,

x2q, ..., xnq, respectively. A quiescent VDDq power supply 110 provides power to the header devices H1q, H2q, ..., Hnq via a VDDq power distribution grid/bus 112. As detailed below, the incorporation of the quiescent power system 104 into the voltage island system 100 allows different circuitry (e.g., voltage islands V1, V2, ..., Vn) to be selectively and/or independently connected to either VDDq or VDDg during testing (e.g., IDDQ testing). Test pattern(s) 120 are provided to the plurality of voltage islands V1, V2, ..., Vn by a tester (not shown) during testing.

[00024] As shown in FIG. 2, the plurality of voltage islands V1, V2, ..., Vn can be selectively connected to a plurality of independent power supplies (i.e., the global VDDg power supply 106 and the quiescent VDDq power supply 110 in this embodiment) using independently controlled connections. To this extent, power can be selectively routed via header control signals x1, x2, ..., xn or header control signals x1q, x2q, ..., xnq to none, some, or all of the plurality of voltage islands V1, V2, ..., Vn. Thus, in the embodiment of the present invention illustrated in FIG. 2, each of the plurality of voltage islands V1, V2, ..., Vn can be selectively powered by either the global VDDg power supply 106 or the quiescent VDDq power supply 110, both power supplies 106, 110, or neither power supply 106, 110. The VDDg and VDDq power supplies output the same voltage (i.e., VDDg = VDDq) to the plurality of voltage islands V1, V2, ..., Vn .

[00025] In the present invention, the quiescent VDDq power supply 110 and VDDq power distribution grid 112 are configured to provide a voltage VDDq and some small amount of current to the plurality of voltage islands V1, V2, ..., Vn when the quiescent VDDq power supply 110 is connected to the plurality of voltage islands V1, V2, ..., Vn. The quiescent VDDq power supply 110 and VDDq power distribution grid/bus 112 do not need to be as robust as the global VDDg power supply 106 and VDDg power distribution grid/bus 108. Accordingly, the quiescent VDDq power supply 110 and VDDq power distribution grid/bus 112 can take up less real estate on the integrated circuit chip on which the voltage island system 100 is formed. In addition, the quiescent VDDq power supply 110 and VDDq power distribution grid/bus 112

can have a greater resistance than the global VDDg power supply 106 and VDDg power distribution grid/bus 108. Advantageously, this greater resistance of can be used, as detailed below, to locate IDDQ defects within the voltage island system 100.

[00026] The plurality of voltage islands V1, V2, ..., Vn can be hot-switched between the global VDDg power supply 106 and the quiescent VDDq power supply 110 to selectively apply a voltage of either VDDg or VDDq (VDDq = VDDg) to each of the plurality of voltage islands V1, V2, ..., Vn. This is illustrated in FIG. 3, where the plurality of voltage islands V1, V2, ..., Vn are powered (indicated by thick lines) by the global VDDg power supply 106 (the quiescent VDDq power supply 110 is disconnected), and in FIG. 4, where the plurality of voltage islands V1, V2, ..., Vn are powered (indicated by thick lines) by the quiescent VDDg power supply 110 (the global VDDg power supply 106 is disconnected). Thus, the plurality of voltage islands V1, V2, ..., Vn always remain powered to substantially the same voltage level by either the global VDDg power supply 106 or the quiescent VDDq power supply 110 and, accordingly, none of the plurality of voltage islands loses state. As such, a test pattern 120 can be applied a single time to the plurality of voltage islands V1, V2, ..., Vn, and different sets of the plurality of voltage islands V1, V2, ..., Vn can be tested (e.g., IDDq testing) when powered by VDDg or VDDq (the test pattern 120 does not have to be reapplied (i.e., the test pattern remains valid) as would be required in the voltage island system 10 of the prior art).

[00027] It should be noted that, in some cases, both the global VDDg power supply 106 and the quiescent VDDq power supply 110 can be turned on at the same time to selectively supply a voltage of either VDDg or VDDq (VDDq = VDDg) to each of the plurality of voltage islands V1, V2, ..., Vn in dependence of the activation/deactivation of the header devices H1, H2, ..., Hn and H1q, H2q, ..., Hnq. This is illustrated in FIGS. 5 and 6. In this example, the hot-switching is controlled by the header devices H1, H2, ..., Hn and H1q, H2q, ..., Hnq (assuming that the global VDDg power supply 106 and the quiescent VDDq power supply 110 are both on). In particular, as shown by the thick lines

in FIG. 5, header device H1 is activated by control signal x1 to supply a voltage VDDg to voltage island V1, header device Hn is activated by control signal xn to supply a voltage VDDg to voltage island Vn, and header device H2q is activated by control signal x2q to supply a voltage VDDq to voltage island V2. The remaining voltage islands (not shown) are similarly provided with a voltage of VDDg or VDDq.

[00028] In FIG. 6, the voltage applied to each of the plurality of voltage islands V1, V2, ..., Vn, has been hot-switched from VDDg to VDDq, or from VDDq to VDDg. In particular, as shown by the thick lines in FIG.6, header device H2 is activated by control signal x2 to supply a voltage VDDg to voltage island V2, header device H1q is activated by control signal x1q to supply a voltage VDDq to voltage island V1, and header device Hnq is activated by control signal xnq to supply a voltage VDDq to voltage island Vn. The remaining voltage islands (not shown) are similarly provided with a voltage of VDDg or VDDq. In each case, the plurality of voltage islands V1, V2, ..., Vn always remain powered up to the same voltage (VDDq = VDDg) and retain state.

[00029] In FIG. 5, a test pattern 120 can be applied to the plurality of voltage islands V1, V2, ..., Vn, while IDDQ testing is performed only on a subset of the voltage islands. For example, let us assume that IDDQ testing is performed only on voltage islands V1 and Vn in FIG. 5, which are powered by VDDg. Instead of turning the remaining voltage islands (i.e., V2, V3, ...Vn-1) off, as would be the case in the voltage island system 10 shown in FIG. 1, resulting in the remaining voltage islands losing state, these voltage islands are instead selectively connected to VDDq. Continuing this example with reference to FIG. 6, let us assume that IDDQ testing is subsequently performed only on voltage islands V2, V3, ...Vn-1, which are now powered by VDDg instead of VDDq (i.e., hot-switching has occurred). Since the voltage islands V2, V3, ...Vn did not lose state during the hot-switching process, the test pattern 120 does not have to be reapplied, as would be the case in the voltage island system 10 illustrated in FIG. 1, thus improving the time efficiency of the IDDQ testing.

[00030] Hot-switching between the global VDDg power supply 106 and the quiescent VDDq power supply 110, and/or between the voltages VDDg and VDDq, provides several advantages. For example, since the plurality of voltage islands V1, V2, ..., Vn are not powered down during the hot-switching process (i.e., the plurality of voltage islands V1, V2, ..., Vn will either be powered by VDDg or VDDq at all times), many IDDQ-type measurements can be made with the same test pattern and chip conditioning, providing more test flexibility and ensuring consistency between measurements. This is in contrast to the voltage island system 10 of FIG. 1, wherein the same test pattern must be reapplied by the tester each time and a different set of the voltage islands V1, V2, ..., Vn is tested. The reapplication of the test pattern is necessary in the prior art voltage island system 10 because the state of a voltage island, when disconnected from a power supply, decays with some RC time constant. In contrast, in accordance with the present invention, the plurality of voltage islands V1, V2, ..., Vn always remain powered, either by a voltage VDDg or VDDq (or both in some cases). It should be noted that hot switching in the present invention is performed at a speed sufficient to prevent the state of any voltage island from decaying to a point where the voltage island loses state.

[00031] Although shown as comprising two power supplies, i.e., the global VDDg power supply 106 and the quiescent VDDq power supply 110, it should be clear that the voltage island system 100 may include more than two power supplies coupled to the plurality of voltage islands V1, V2, ..., Vn. In addition, the selective application of voltage to the plurality of voltage islands V1, V2, ..., Vn can be provided using means other than header devices. It should also be noted that VDDq could be designed so that it is separate during IDDQ testing and becomes part of functional power for other testing and functional operations.

[00032] The voltage island system 100 of present invention provides numerous advantages over the prior art. The advantages include, for example,: a) voltage island specific IDDQ measurements can be made by reconfiguring

voltage island power connects (i.e., via header control signals x1, x2, ..., xn, x1q, x2q, ..., xnq) for IDDQ measurements; b) allows part disposition based on comparison of IDDQ measurements and calculated IDDQ, such as comparing the IDDQ for two instances of the same voltage island on a device; c) by reducing the amount of circuitry connected to power (or ground) during IDDQ measurement, the background leakage current is less, resulting in a higher IDDQ signal-to-noise ratio; d) IDDQ measurements can be used to detect and locate an IDDQ defect - resolution depends on granularity of voltage islands, background leakage current, and tester current measurement capability; e) routing between separate power supplies allows voltage islands to stay powered up and retain valid state; f) hot switching allows test pattern conditioning to be separated from voltage island connection configuration with appropriate logic included in the semiconductor device to allow voltage island connection changes independent of device conditioning; g) saves test pattern application time and complexity, ensures consistency between measurements, and facilitates search algorithms; h) global circuitry and voltage island circuitry can be separated, allowing direct measurements of IDDQ for voltage islands, and direct measurement of IDDQ for the global circuitry without disconnecting all the voltage islands from power; i) can collect IDDQ measurements from both the global voltage supply VDDg and the quiescent voltage supply VDDq at the same time (if have different external power supplies); j) because the quiescent power supply VDDq does not need to supply large amounts of current and only holds the voltage (DC supply) during IDDQ measurement, the quiescent power supply VDDq does not have to be as robust as the global power supply VDDg. Also, the VDDq power distribution grid/bus can be more resistive than the device operational power grids, as can the connection circuitry, although this does not have to be the case; k) allows current measurement with all voltage islands disconnected from the quiescent power supply VDDq; l) the quiescent power supply VDDq can be combined with on-chip voltage sensors to monitor voltage at many locations inside the chip on the VDDq power distribution grid/bus, allowing many voltage measurements at once, and moving the measurements to the device, reducing acquisition time and required equipment needed to make current measurements; m) connections to the quiescent VDDq

power supply need not be the same as those used for functional power management and, as such, they could be optimized for test; n) IDDQ can be measured for each different connection configuration between the plurality of voltage islands and the power supplies. This could provide an enhanced method of testing, depending on how the power supply connections are implemented. These IDDQ measurements could be compared with a threshold or compared against each other if appropriate for the design; o) the invention structure can be used with standard IDDQ testing (e.g., where the IDDQ value is compared against a threshold), delta IDDQ testing (where the distance between an IDDQ measurement and a previous IDDQ measurement is compared to a threshold, i.e., +/- 10%), and other more complex schemes, for example, where device IDDQ measurements are compared to sliding thresholds based on other standard measurements taken from the device, such as ring oscillator frequencies; p) the invention enables the use of another class of IDDQ test algorithms that use the IDDQ measurements from individual voltage islands or groups of islands to test the chip. For example, the IDDQ measurement for an individual voltage island or group of voltage islands could be compared with that of another instance of the same circuitry on the same chip, or IDDQ current measurements for each voltage island could be compared to the average measurement for all the voltage islands on a particular chip. In this way, variation amongst instances of the same circuitry could be measured, and individual measurements could be "normalized" for the background current of the device. These IDDQ measurements could also be used to compare between neighboring chips for statistical device dispositioning; q) on-chip voltage sensors could be used to test the device by locally thresholding, on-chip comparison of voltage levels, or downloading IDDQ measurements; and r) the voltage island system 100 can be used in an on-chip IDDQ BIST implementation.

[00033] The voltage island system 100 of the present invention enables use of automatic tester diagnostics to identify failing voltage island(s), using search schemes, such as binary search, to optimize search time, number of IDDQ measurements, power connection configurations, and number of test

pattern iterations. Diagnostics and localization can be performed to varying degrees depending on the application. For example, IDDQ measurements for specific voltage island(s) can be cross-referenced to the physical location of the voltage island(s) and a map created. IDDQ maps provide a physical correlation to defect location (defect, source or sink), and can be used for yield analysis and to determine common fail signatures, as well as provide initial defect location estimates for hardware fault isolation techniques. The possible physical granularity of the IDDQ map depends on the granularity of the control logic and physical extent of each voltage island. Physical information in IDDQ maps can be used to differentiate between multiple defects on one chip by location and pattern (if more than one map). Further, on-chip voltage sensors may be used to provide pass/fail or voltage information. Voltage sensor locations can be cross-referenced to physical locations on the VDDq power distribution grid/bus and in the device, and a map created. Voltage maps can be used in the same applications as IDDQ maps. In addition, for finer diagnostics/localization, IDDQ measurements, results from test comparisons, and IDDQ current maps can be used to provide input to IDDQ software diagnostics. Voltage sensor measurements and VDDq conductance can also be used to locate an IDDQ defect. Measurements at multiple points on the VDDq power distribution grid/bus can improve detection and resolution of the IDDQ defects. Maps of VDDq conductance isobars can be used to triangulate the defect location.

[00034] The quiescent power system 104 of the present invention may also be used as a power monitor for power testing. This could be done at any level, for example, wafer test, packaged test, system test, and in the field. Basically, after a desired set of voltage islands are hot-switched onto the VDDq power distribution grid/bus 112 (i.e., connected to VDDq), the device is tested/operated, and the VDDq power supply 110 current/ power (P=VI) is monitored. Power can be monitored when the device is in the quiescent state. During other testing and functional operation of the device, power can be monitored within the design constraints of the VDDq bus.

[00035] Another embodiment of a voltage island system 200 in accordance with the present invention is illustrated in FIG. 7. Similar to the voltage island system 100 shown in FIG. 2, the voltage island system 200 includes a plurality of voltage islands V1, V2, ..., Vn, a global power system 202, and a quiescent power system 204. The global power system 202 includes a first plurality of on-chip header devices H1, H2, ..., Hn for selectively providing a voltage VDDg to the plurality of voltage islands V1, V2, ..., Vn in response to first header control signals x1, x2, ..., xn, respectively. A global VDDg power supply 206 provides power to the header devices H1, H2, ..., Hn via a VDDg power distribution grid/bus 208. The quiescent power system 204 includes a second plurality of on-chip header devices H1q, H2q, ..., Hnq for selectively providing a quiescent voltage VDDq to the plurality of voltage islands V1, V2, ..., Vn in response to second header control signals x1q, x2q, ..., xnq, respectively, and a third plurality of on-chip header devices H1'q, H2'q, ..., Hn'q for selectively providing the quiescent voltage VDDq to the plurality of voltage islands V1, V2, ..., Vn in response to third header control signals x1'q, x2'q, ..., xn'q, respectively. A quiescent VDDq power supply 210 provides power to the header devices H1q, H2q, ..., Hnq via a VDDq power distribution grid/bus 212. The quiescent power system 204 also includes a plurality of voltage sensors 214, each located on a connection between the plurality of voltage islands V1, V2, ..., Vn and the header devices H1q, H2q, ..., Hnq and H1'q, H2'q, ..., Hn'q.

[00036] Locating the voltage sensors 214 on-chip provides many advantages over off-chip voltage measurements (e.g., at the tester). For example, voltage measurements can be made more quickly when the voltage sensors 214 are located on-chip. In addition, voltage measurements may be made in parallel on the plurality of voltage sensors 214 rather than one at a time, as would be the case where voltage measurements are made at the tester. Testing granularity can also be adjusted, based on the number/density of voltage sensors 214 that are used. For example, a greater number of voltage sensors 214 may be located in areas of a chip that are more susceptible to IDDQ defects, while a lesser number of voltage sensors 214 may be placed in other areas of the chip.

[00037] In FIG. 7, the plurality of voltage sensors 214 are shown located outside of the plurality of voltage islands V1, V2, ..., Vn. However, the plurality of voltage sensors 214 should be placed for optimal defect detection, which depends on how VDDq is implemented. For example, as shown in FIGS. 8A and 8B, an IDDq defect 220 may be detected by placing voltage sensors 214a, 214b, 214c, and 214d on VDDq conductive paths 222a, 222b, 222c, and 222d, respectively, (e.g., conductive paths to voltage islands or other circuits) and applying a test voltage V to the VDDq rail 224. When no IDDq defect exists as shown in FIG. 8A, then all of the voltage sensors 214a, 214b, 214c, and 214d see the voltage V applied to the VDDq rail 224 (ignoring background leakage). However, when an IDDq defect 220 exists, as shown in FIG. 8B, then voltage sensors 214a, 214c, and 214d see a voltage substantially equal to V, while voltage sensor 214b sees a voltage V_{214b} equal to $R_{metal}/R_{defect} * V$, where R_{metal} is the resistance of the metal forming the conductive path 222b and R_{defect} is the resistance of the IDDQ defect 220. Thus, in this case, the voltage sensors 222a, 222c, and 222d see a voltage of approximately V, while the voltage sensor 22b sees a voltage less than V (depending on the ratio of R_{metal}/R_{defect}).

[00038] The foregoing description of various aspects of the invention has been presented for purposes of illustration and description. It is not intended to be exhaustive or to limit the invention to the precise form disclosed, and obviously, many modifications and variations are possible. Such modifications and variations that may be apparent to a person skilled in the art are intended to be included within the scope of the invention as defined by the accompanying claims. For example, the present invention can be applied to ground GND instead of VDD. Such a system would include a global ground bus and a quiescent ground bus, wherein current measurements are taken on separate ground supplies.

INDUSTRIAL APPLICABILITY

[00039] The invention is useful for integrated circuit testing. More particularly, the present invention provides a voltage island system including a hot-switchable voltage bus for IDDQ current measurements.